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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/539,224
Filing Date: June 16, 2005
Appellant(s): VENEZIA ET AL.

Vincent Venezia
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 08/13/2009 appealing from the Office action mailed 01/28/2009.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6074922	Wang et al.	06-2000
20010003056	Hashimoto	06-2001
6,348,390	Wu	02-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,2 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al.(US 6,074,922).

Re. claim 1, Wang et al. discloses a method of manufacturing a semiconductor device with a semiconductor body of a semiconductor material, the semiconductor device including field effect transistor having a source and drain region at a surface of the semiconductor body, and having a gate region between the source and drain region , the gate region including a semiconductor region of a further semiconductor material that is separated from the surface of the semiconductor body by a gate dielectric, the method comprising: forming a gate dielectric (14) on the surface of the semiconductor substrate(same as semiconductor body)(10); forming a semiconductor region (16) on the gate dielectric (14); depositing a sacrificial region(30) on top of the semiconductor region(16); after depositing the sacrificial region(30), forming spacers(34) adjacent to the gate region for forming the source and drain regions; forming the source and drain

regions(36) on the surface of the semiconductor body ; after forming the source and drain regions, selectively etching the sacrificial region(30) with respect to the semiconductor region; depositing a metal layer (40) on the source region, drain region, and the gate region(Figure 6); forming a compound(42) that includes at least a portion of the source and drain regions, of the metal layer and the semiconductor material(Note: the metal is on the portions of the source and drain which makes the source and drain portions with metal and so the limitation of claim for forming the compound that includes at least a portion of the source and drain regions of the metal layer and the semiconductor material) ; and forming a compound that includes at least a substantial portion of the further semiconductor material, of the metal layer and further semiconductor material(Figure 8).

Re. claim 2, Wang et al. discloses having the sidewall spacers(same as spacers)(34) formed by depositing a layer of dielectric material on top of the substrate on which the gate region comprising the conductive layer(16) and the dielectric layer(same as sacrificial region) (30) is present and by subsequently removing the deposited layer on top of and on both sides of the gate region by etching (Column 3,line 53-57).

Re. claim 10, Wang et al. discloses a semiconductor device comprising a field effect transistor obtained by a method as claimed in any of the preceding claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Wang et al.(US 6,074,922) in view of Hashimoto(US 2001/0003056).

Re. claim 3, Wang et al. discloses all the limitations except having the semiconductor region completely consumed during the formation of the compound of the metal and the further semiconductor material.

However, Hashimoto discloses having gate electrode(120)(same as semiconductor region) completely consumed during the formation of the CoSi.sub.2 layer(same as compound)of the metal layer and the further semiconductor material(Para[0096],line 1-2).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Wang et al. as taught by Hashimoto to have the semiconductor region completely consumed during the formation of the compound of the metal and the further semiconductor material to minimizes the wiring resistance of the gate electrode (Para[0094],line 4-5).

Re. claim 4, Wang et al. discloses all the limitations except the limitations disclosed in claim 4. However, Hashimoto teaches the formation of the CoSi.sub.2 layer(same as compound) between the metal and the semiconductor material and the metal and the

further semiconductor material is carried out in two separate heating steps, the first heating step resulting in an intermediate compound with a low content of the semiconductor material or of the further semiconductor material and in the second heating step the intermediate compound being converted to the compound having a higher content of the semiconductor material or of the further semiconductor material(Para[0096]).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Wang et al. as taught by Hashimoto to have the formation of compound with two step heating to have he surface portion of the Co.sub.2Si layer or CoSi layer prevented from being exposed during the high-temperature reaction and is therefore silicon-rich so that the surface energy of the Co.sub.2Si layer or CoSi layer is lower than in the conventional embodiment. As a result, agglomeration is less likely to occur at the surface of the Co.sub.2Si layer or CoSi layer so that a gate electrode composed of the CoSi.sub.2 layer with good uniformity in reaction thickness is formed(Para [0097].

Re. claims 5, Wang et al. discloses all the limitations except the limitations disclosed in claim 5.

However, Hashimoto teaches that between the two heating steps, a part of the cobalt film (same as metal layer) which has not reacted to form the intermediate compound is removed by etching (Para [0073],line 6-9).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Wang et al. as taught by Hashimoto to have cobalt film (same as metal layer) which has not reacted to form the intermediate compound is removed by etching so that agglomeration is less likely to occur at the surface of the Co.sub.2Si layer or CoSi layer so that a gate electrode composed of the CoSi.sub.2 layer with good uniformity in reaction thickness is formed([Para[0097]).

Re. claim 6, Wang et al. discloses all the limitations except the limitations disclosed in claim 6.

However, Hashimoto teaches having a silicon film(same as layer)of the further semiconductor material is deposited on the surface of the gate electrode(same as semiconductor body).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Wang et al. as taught by Hashimoto to have a layer deposited on

the surface of the gate electrode to minimizes the wiring resistance of the gate electrode (Para[0094],line 4-5).

Re. claim 7, Wang et al. discloses all the limitations except the limitations disclosed in claim 7. However, Hashimoto teaches that after the second heating step, a part of the silicon film(same as layer)of the further semiconductor material which has not reacted to form the compound is removed by etching(Para[0080],line1-3).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Wang et al. as taught by Hashimoto a part of the silicon film(same as layer)of the further semiconductor material which has not reacted to form the compound is removed by etching to achieve a higher speed operation and low power consumption(Para[0089],line 15-16).

Re. claim 9 as discussed above in claim 4, Wang et al. and Hashimoto discloses semiconductor material chosen is silicon (column 3,line 11-13), and for the metal silicide layer(same as compound)(42) for the compound of the metal and the semiconductor material and the further semiconductor material a metal silicide is chosen(column 4,line 1-8, Wang et al.).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al.(US 6,074,922) in view of Wu(US 6,348,390).

Re. claim 8 as discussed above in claim 1, Wang et al. discloses all the limitations as discussed above in claim 1 except after the formation of the compounds of the metal and the semiconductor material and of the metal and the further semiconductor material, the spacers are removed.

However, Wu discloses after the formation of the metal silicide layer(same as compound)(28) of the metal and semiconductor material(column 5,line 54-58), the spacers(22) are removed(Column 6,line 1-2) to form extended source/drain region.

Therefore it would have been obvious for one with ordinary skill in the art at the time the invention was made to provide Wang et al. structure with method of removing spacer of Wu et al. to form extended source/drain region.

(10) Response to Argument

I(issue): **The Rejection Of Claims 1-2 And 10 Under U.S.C. § 102(b) Over The '922 Reference Should Be Reversed Because The '922 Reference Fails To Disclose That A Layer Of Semiconductor Gate Material Is Substantially Transformed Into Compound Of Semiconductor And Metal Material .**

(a) To sustain a § 102 rejection, each and every claim element must be taught by the applied reference. Appellant submits that the '922 reference clearly fails to meet this

standard because the '922 reference does not disclose forming a compound, that includes at least a substantial portion of the further semiconductor material *(i. e.,* the gate region), of the metal layer and the further semiconductor material. Rather, the '922 reference teaches that silicide 42 *(i. e.,* the asserted compound) is formed on top of polysilicon gate *16 (i. e.,* the asserted further semiconductor material) from titanium layer 40 *(i. e.,* the asserted metal layer). *See, e.g.,* Figures 6-8.

R(Response):

Issue(a):

In response to appellant's arguments for claims 1-2 and 10, "...Appellant submits that the '922 reference clearly fails to meet this standard because the '922 reference does not disclose forming a compound, that includes at least a substantial portion of the further semiconductor material *(i. e.,* the gate region), of the metal layer and the further semiconductor material...", The term salicide from the title of Wang et al.(US 6,074,922) refers to a technology used in the microelectronics industry used to form electrical contacts between the semiconductor device and the supporting interconnect structure. The salicide process involves the reaction of a thin metal film with silicon in the active regions of the device, ultimately forming a metal silicide contact through a series of annealing and/or etch processes. The term "salicide" is a compaction of the phrase self-aligned silicide. The description "self-aligned" suggests that the contact formation does not require lithographic patterning processes and in Wang et al. the

metal (40) is deposited on the semiconductor material (16)(i.e. polysilicon) as shown in figure 6 and thereafter in figure 7 a series of annealing processes as mentioned in the salicide process will lead to transformation of the semiconductor layer into metal silicide based on the definition of salicide and will make the Wang et al. reference read on the "...forming a compound, that includes at least a substantial portion of the further semiconductor material *(i. e.,* the gate region), of the metal layer and the further semiconductor material... " limitation .

I(issue): **The Rejections Of Claims 3-7 And 9 Under U.S.C. § 103(a) Over The '922 Reference In View Of The '056 Reference Should Be Reversed Because There Is No Motivation For The Skilled Artisan To Modify The '922 Reference In The Manner Proposed By Examiner**

The Rejection Of Claim 3 Under U.S.C. § 103(a) Over The '922 Reference In View Of The '056 Reference Should Be Reversed Because There Is No Motivation For The Skilled Artisan To Modify The '922 Reference In The Manner Proposed By Examiner .

In response to appellant's arguments for claims 3-7 and 9 "...claim 3 recites "further semiconductor region is completely consumed during the formation of the compound of the metal layer and the further semiconductor material." Appellant disagrees and submits that the skilled artisan would not be motivated to implement such a modification of the '922 reference in part because the modification attempts to solve a problem that is not present in the cited embodiment and because the modification drastically alters the entire process and structure taught by the '922 reference. ..." , the Wang et al. teaches enhanced structure for salicide mosfet, in which the salicide involves the reaction of a thin metal film with silicon in the active regions of the device, ultimately forming a metal silicide contact through a series of annealing and/or etch processes which leads to transformation of semiconductor region(16) to metal silicide but since the Wang et al. reference does not provide proper figures to show the exact salicide process the Examiner has provided the Hashimoto(US 2001/0003056) reference to make it more clear for the Appellant and based on these reasoning's the combination of Wang et al. and Hashimoto is proper because from the salicide it involves the reaction of a thin metal film with silicon in the active regions of the device, ultimately forming a metal silicide contact through a series of annealing and/or etch processes and even though Wang et al. just transforms substantial portion of the semiconductor region (16) into metal silicide, the further annealing of Hashimoto will completely consume the semiconductor region into a compound.

In response to appellant's arguments for claims 3-7 and 9 "...Logic dictates that the steps of the primary reference would not be obvious to implement only to then undo the very reasons for why the skilled artisan would seek to perform the original steps. Rather than producing a device having an increased salicide thickness and effective polysilicon thickness *(see, e.g.,* '922 reference, Abstract), the proposed modification completely removes the polysilicon. Accordingly, the rejection violates M.P.E.P. § 2143.01. *See also In re Gordon,* 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984) (A §103 rejection cannot be maintained when the asserted modification undermines the purpose of the main reference)...", the way the 103 rejection is used is that taking figure 8 of Wang et al. and forming a silicon layer and annealing of Hashimoto will completely consume the semiconductor and transform into a compound .

I(Issue): **The Rejection Of Claims 4-7 And 9 Under U.S.C. § 103(a) Over The '922 Reference In View Of The '056 Reference Should Be Reversed Because There Is**

No Motivation For the Skilled Artisan To Modify The '922 Reference In The Manner Proposed By The Examiner .

(a) The Examiner's proposed modification of the '922 reference to use the two step heating process of the '056 reference undermines the purpose and operation of the '922 reference. *See, e.g.,* M.P.E.P. § 2143.01 and also *In re Gordon,* 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984) (A § 103 rejection cannot be maintained when the asserted modification undermines the purpose of the main reference). In this instance, a main objective of the '922 reference is to reduce bridging between the gate and the source/drain. For example, the '922 reference states "The process of the invention provides an effective method of fabricating an integrated circuit device having a silicided polysilicon gate with reduced resistance, increased effective polysilicon width, increased salicide thickness, improved yield, and reduced gate to source/drain bridging." '922 reference, Col. 5:33-37 (emphasis added). Appellant submits that the Examiner's proposed combination would result in the gate being shorted to the source/drain thereby undermining the purpose of the '922 reference.

R(Response):

Issue(a)

In response to appellant's arguments for claims 4-7 and 9 "...**The Examiner's proposed modification of the '922 reference to use the two step heating process of the '056 reference undermines the purpose and operation of the '922 reference. *See, e.g.,* M.P.E.P. § 2143.01 and also *In re Gordon,* 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984) (A § 103 rejection cannot be maintained when the asserted modification undermines the purpose of the main reference). In this instance, a main objective of the '922 reference is to reduce bridging between the gate and the source/drain. For example, the '922 reference states "The process of the invention provides an effective method of fabricating an integrated circuit device having a silicided polysilicon gate with reduced resistance, increased effective polysilicon width, increased salicide thickness, improved yield, and reduced gate to source/drain bridging." '922 reference, Col. 5:33-37 (emphasis added). Appellant submits that the Examiner's proposed combination would result in the gate being shorted to the source/drain thereby undermining the purpose of the '922 reference.." In contrast, the '922 reference transforms the titanium layer 40 into titanium silicide 42 while avoiding transformation or consumption of its gate electrode 16. *See, e.g.,* Figures 6-7 and Col. Col. 3:59 to Col. 4:15. Apparently recognizing this issue, the Examiner proposes that the prior art would lead a skilled artisan to modify the teaching of the '922 reference by the '056 reference's teaching that, for a certain embodiment in the '056 reference, the'056 reference's gate can be consumed as part of its semiconductor manufacturing process**..." the Wang et al. teaches enhanced structure for salicide mosfet, in which the salicide

involves the reaction of a thin metal film with silicon in the active regions of the device, ultimately forming a metal silicide contact through a series of annealing and/or etch processes which leads to transformation of semiconductor region(16) to metal silicide so heating of the Wang et al. reference to a certain level can read on the claim limitation of forming a compound includes a substantial portion of the further semiconductor material read on the prior art and thereafter removing the unreacted metal and then forming a silicon layer of Hashimoto(Para[0096]) over the titanium silicide(42) of figure 8 of Wang et al. and then performing a second heat treatment so that the gate is completely consumed with titanium silicide, however Appellant interpretation of using figure 7 and then applying a silicon layer and then heat treatment is wrong because that will lead to short circuit, therefore for the appropriate 103 rejection the examiner has used figure 8 of Wang et al. and then applying a silicon layer on figure 8 and then performing a second treatment of Hashimoto to completely consume the gate of Wang et al. with titanium silicide as a result agglomeration is less likely to occur at the surface of the Ti.sub.2Si layer or TiSi layer so that a gate electrode composed of the TiSi.sub.2 layer with good uniformity in reaction thickness is formed.

I(Issue): **The Rejection Of Claim 8 Under U.S.C. § 103(a) Over The '922 Reference In View Of The '390 Reference Should Be Reversed Because No Valid Reason Has Been Presented To Modify The '922 Reference**

(a) In regard to claim 8, the Examiner acknowledges that the'922 reference does not teach removing spacers 34. The Examiner then asserts that the skilled artisan would modify the'922 reference to remove the spacers 34 as taught by the '390 reference in order "to form extended source/drain regions." The '922 reference, however, already teaches that lightly doped source and drain regions 32 *(i. e.,* extended source/drain regions) are formed prior to the formation of the spacers 34. *See, e.g.,* Figures 2-4 and Col. 3:35-36. Appellant submits that the Examiner's alleged motivation for the proposed combination is based on a nonexistent problem that has already been addressed by the '922 reference. Accordingly, the Examiner has not provided any evidence as to why one of skill in the art would find the asserted combination obvious as required.

R(Response):

Issue(a)

In response to appellant's arguments for claim 8, " ... the Examiner acknowledges that the'922 reference does not teach removing spacers 34. The Examiner then asserts that the skilled artisan would modify the'922 reference to remove the spacers 34 as taught by the '390 reference in order "to form extended source/drain regions." The '922 reference, however, already teaches that lightly doped source and drain regions 32 *(i. e.,* extended source/drain regions) are formed prior to the formation of the spacers 34. *See, e.g.,* Figures 2-4 and Col. 3:35-36. Appellant submits that the Examiner's alleged motivation for the proposed combination is based on a nonexistent problem that has

already been addressed by the '922 reference. Accordingly, the Examiner has not provided any evidence as to why one of skill in the art would find the asserted combination obvious as required...", the Wu reference discloses after the formation of the metal silicide layer(same as compound)(28) of the metal and semiconductor material(column 5,line 54-58), the spacers(22) are removed(Column 6,line 1-2) to form extended source/drain region, the extended portion does not only need to be a lightly doped region and highly doped region it can also be halo or pocket region.

(11) Related Proceeding(s) Appendix

None

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/A. k. S./

Examiner, Art Unit 2895

Conferees:

Mr. Drew N. Richards /Matthew S. Smith/ for Drew Richards

Supervisory Patent Examiner, Art Unit 2895

Mr. David Porta /David P. Porta/

Supervisory Patent Examiner, Art Unit 2884